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ION IMPLANTED GaAs I.C. PROCESS TECHNOLOGY

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Prepared by:

D.R. Ch'en
Principal Investigator

F.H. Eisen
Co-Principal Investigator

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This report covers the first quarter, Phase II of a program on ion implanted planar GaAs integrated circuit technology. The overall objective of this program is the development of a manufacturable process for high-speed low-power GaAs logic circuits. The goal for Phase I was to establish the technology, and demonstrate its viability by fabricating circuits reaching MSI complexity. The goal for Phase II is to achieve the capability of fabricating GaAs ICs of LSI complexity. The program involves the Rockwell International Science Center and three subcontractors; Crystal Specialties Inc ,

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California Institute of Technology and Cornell University.

The most important result obtained in this quarter is the verification of proper operation of an 8-channel multiplexer. This multiplexer, employing 64 gates, is the most complex GaAs IC built to date. The first multiplexer results show operation at "moderate" speed, 254 MHz clock rate with low power dissipation, 80 mW, for the entire circuit. Testing of wafers which are expected to demonstrate operation at higher speed is in progress.

Work on all other related aspects of the program has continued. The procedure for preselecting substrates has been streamlined. Study of silicon implantation for achieving high electron concentrations has continued. Encouraging results on circuit fabrication have been obtained from an ion milling procedure for the second layer metalization. After preliminary tests, some wafers have been processed employing this technique for the second layer metalization, and it is anticipated that all wafers will be processed this way in the future.

Statistical analysis of data from test FETs obtained with our automatic measurement system shows strong correlations between saturation current and pinchoff voltage. This is an indication of tight control on process variables. National Bureau of Standards (NBS) test patterns for the measurement of sheet resistance and line width, and for electrical verification of alignment between mask steps have been tested with satisfactory results.

Design work has started on a third mask set. It will contain circuits with increased complexity over AR2, including a 3 x 3 binary multiplier and large multiplexer containing more than 100 gates.

FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Science Center as the prime contractor with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Materials Science Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. The Rockwell program manager is Fred A. Blum. The principal investigators for each organization are:

Science Center	F. H. Eisen, D. R. Ch'en
California Institute of Technology	J. W. Mayer, M. A. Nicolet
Cornell University	L. F. Eastman
Crystal Specialties	W. P. Allred

Numerous other researchers are involved in the work reported on. The principal contributors are:

Science Center	P. Asbeck, R. Eden, R. D. Fairman, F. S. Lee, S. I. Long, F. J. Morin Y. D. Shen, B. M. Welch R. Zucca
California Institute of Technology	A. Masuyama
Cornell University	M. Shur
Crystal Specialties	J. Burns, H. Olsen

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TECHNICAL SUMMARY

This report covers the first quarter, Phase II of a program on ion implanted planar GaAs integrated circuit technology. The goal for the second phase of the program is to achieve the capability of fabricating GaAs ICs of LSI complexity. The fabrication approach, demonstrated in Phase I, is based on multiple localized implantations directly into the semi-insulating GaAs substrate to form active device areas insulated by the unimplanted regions of the substrate. The circuit concept, also demonstrated in Phase I, involves a combination of Schottky diodes and depletion mode Schottky barrier FETs (SDFL), employed to form logic gates capable of high speed operation with very low power.

This program requires a research effort on all the multiple facets of process development. The research activities range from substrate growth and ion implantation technology to fabrication and evaluation of test circuits. These activities are carried out by the Science Center with the support of three subcontractors, Cal Tech, Cornell University, and Crystal Specialties, Inc.

The following is a summary of the accomplishments of the program in the past quarter.

Semi-insulating Substrate Material (Section 2)

Crystal Specialties has continued supplying the qualified semi-insulating substrate material required by the program. Appearance of

inclusions in the ingots was traced to gallium richness of the melts used, and eliminated. An added feature was incorported in the routine procedure used in selecting ingots suitable for the IC process. This feature consists of the implantation of Se^+ ions at doses representative of the IC process, and subsequent examination of the doping profile with the C-V technique. This test serves as a confirmation on substrate quality, and it also provides information on the Se^+ dose most suited to a particular substrate. Preliminary measurements by photo-induced transient spectroscopy (PITS) on substrates that underwent various thermal treatments, indicate that the technique is very sensitive to such process variable.

Planar Process Development (Section 3)

The study of silicon implantation as a means of achieving high doping density in GaAs with a process compatible with the low dose implantations has continued. Processing of IC wafers employing mask set AR2 has continued, providing more wafers for the evaluation of the MSI demonstration circuit contained in this mask set. Considerable effort has gone into characterizing the dry etching process for a second layer metallization. This process employs an ion milling technique instead of the currently used photoresist liftoff procedure. The results are quite satisfactory. Consequently, some of the wafers are being processed with the ion milling technique, and it is anticipated that such technique will be exclusively used in the near future.

Circuit Performance (Section 4.1)

Testing of MSI circuits has continued very successfully. Proper operation of a multiplexer employing 64 gates has been demonstrated. This result marks the first time a circuit of this complexity using GaAs Schottky diode FET logic has been in operation. Statistical analysis of test device parameter using the automatic measurement system described in the Annual Report[1] has shown a very strong correlation between saturation current and pinchoff voltage of FETs. This is an indication of tight control on process variables. The evaluation of National Bureau of Standards test patterns (developed for silicon technology) has shown that some of them, such as the sheet resistance, linewidth, and electrical alignment test patterns are applicable to our technology.

Mask Design (Section 4.2)

A new mask set, AR3, is under design. This third mask set will contain circuits with increased complexity over AR2, including a 3 x 3 binary multiplier, and a latched demultiplexer containing more than 100 gates. Based on the experience accumulated from the previous mask sets the process monitor chip is also being redesigned, and the overall mask organization is being restructured.

1.0 INTRODUCTION

This report covers the first quarter, Phase II of a program on ion implanted planar GaAs integrated circuit technology. The objective of this program is the development of an integrated circuit process technology for GaAs taking advantage of its superior electrical properties in order to achieve high speed low power digital integrated circuits. The goal for Phase I was to establish the technology, and demonstrate its viability by fabricating circuits reaching MSI complexity.[1] The goal for Phase II is to achieve the capability of fabricating GaAs ICs of LSI complexity. The bulk of the work on this program is carried out at the Rockwell International Science Center. However, significant assistance is provided by three subcontractors; Crystal Specialties Inc., California Institute of Technology, and Cornell University.

The most important result obtained in this quarter is the verification of proper operation of the 8-channel multiplexer in mask set AR2. This multiplexer, employing 64 gates, is the most complex GaAs IC built to date. The first multiplexer results show operation at "moderate" speed, 254 MHz clock rate with low power dissipation, 80 mW, for the entire circuit. Testing of wafers which are expected to demonstrate operation at higher speed is in progress.

Work on all other aspects of the program has continued. The procedure for preselecting substrates has been streamlined. Study of silicon implantation for achieving high electron concentrations has continued.

Encouraging results on circuit fabrication have been obtained from an ion milling procedure for the second layer metallization. After preliminary tests, some wafers have been processed employing this technique for the second layer metallization, and it is anticipated that all wafers will be processed this way in the future. Ion milling gives better edge definition of the second layer metal lines than lifting. But, most important, ion milling does not limit the thickness of the second layer metallizations to only 2000-3000Å. A 5000-6000Å thick second layer metal will be advantageous as circuit complexity increases requiring the second layer metal power bus lines to carry higher currents.

Statistical analysis of data from test FETs obtained with our automatic measurement system shows strong correlations between saturation current and pinchoff voltage. This is an indication of tight control on process variables. National Bureau of Standards (NBS) test patterns for the measurement of sheet resistance and line width, and for electrical verification of alignment between mask steps have been tested with satisfactory results.

Design work has started on a new mask set, AR3. This third mask set will contain circuits with increased complexity over AR2, including a 3 x 3 binary multiplier and large multiplexer containing more than 100 gates. Based on the experience accumulated from mask sets AR1 and AR2, the process monitor chip, PM, will be redesigned. It will incorporate some NBS test patterns.

2.0 MATERIAL

This section reports on the work carried out at Crystal Specialties on growth of semi-insulating GaAs ingots. The Science Center's evaluation of the material provided by Crystal Specialties, for the IC process is then discussed. Finally, analytical work toward understanding the differences between qualified and unqualified semi-insulating substrates is presented.

2.1 Bulk Growth of Semi-Insulating GaAs (Crystal Specialties)

During this reporting period, the single crystal yield (fraction of growth starts that yielded single crystal ingots) was 92%. This high value reflects the excellent control of boat wetting that has been achieved over the last several quarters.

Many of the ingots grown this quarter were found to contain inclusions. This problem was traced to the use of melts too rich in Ga. Under these circumstances, excess Ga accumulates at the solid-liquid interface and can become trapped in the growing crystal. This result is consistent with previous SIMS observations of inclusions with high Cr content,[2] since, due to the very low Cr distribution coefficient ($\sim 6 \times 10^{-4}$), the included melt is much richer in Cr than the surrounding material. The problem has been rectified by using melts of nearly stoichiometric composition.

2.2 Evaluation of Semi-Insulating Material (Science Center)

An added feature was incorporated in the routine procedures used in selecting ingots suitable for in the IC process. In previous work, two tests have been used for the qualification of ingots: (i) substrates were capped with Si_3N_4, subjected to an annealing cycle (850°C for 30 min) and tested for surface conversion; and (ii) substrates were bombarded with Kr^+ ions, followed by a similar capping and annealing cycle, and conductivity tests. The formation of a conductive surface layer in these tests would disqualify the wafer under examination. In our current routine procedure, both these tests are carried out, and the substrates additionally undergo implantation of Se^+ ions at doses representative of the IC process (2.0×10^{12} cm^{-2} to 2.6×10^{12} cm^{-2}). The capping and annealing procedures are identical to those used for IC fabrication. The carrier profiles produced in the wafer are subsequently examined with the C-V technique. Since the profiles are analogous to those obtained during IC processing, this test provides an additional measure of the substrate quality, which supplements the data of tests (i) and (ii) in the case of marginal ingots. It also provides information on the Se^+ dose most suited to a particular substrate. Our results to date on the ingots subjected to this expanded qualification routine show, as expected, excellent correlation between ingots that pass the two earlier tests and those that provide acceptable Se implant profiles.

During the quarter, 4 ingots grown by Crystal Specialties were submitted to the qualification process; two of these were found acceptable for ion implantation use. In light of the low number of ingots (which reflects

the inclusion problem detailed above), further material must be examined before it can be determined if the qualification yield has increased over previous quarters.

2.3 Material Analysis (Science Center)

The previous annual report described a Photo-Induced Transient Spectroscopy technique, (PITS), developed for the evaluation of trap energies and emission rates in semi-insulating substrate material.[1,3] The technique is being applied to the characterization of substrate material and to the study of how process variables affect a substrate material.

Some preliminary results are shown in Fig. 2.3-1 for a specimen of Morgan Semiconductor substrate and in Fig. 2.3-2 for a specimen of Crystal Specialties substrate. The process variables being studied are the effect of Krypton bombardment plus 850°C anneal and of the 850°C anneal alone. In the figures, the PITS signal has been normalized by dividing it by the steady state photocurrent in order to remove the temperature-dependent lifetime of the carriers. Consequently, the curve is roughly proportional to the product of trap concentration and emission rate. The normalized PITS signal is shown as a function of temperature and also as a function of trap energy determined for an emission cross section of $10^{-13}cm^2$. Also shown is the Fermi level, E_F, calculated for each specimen from its dark conductivity. The letter, I, indicates signal inversion that occurs when the trap cross section is significantly less than the recombination center cross section.

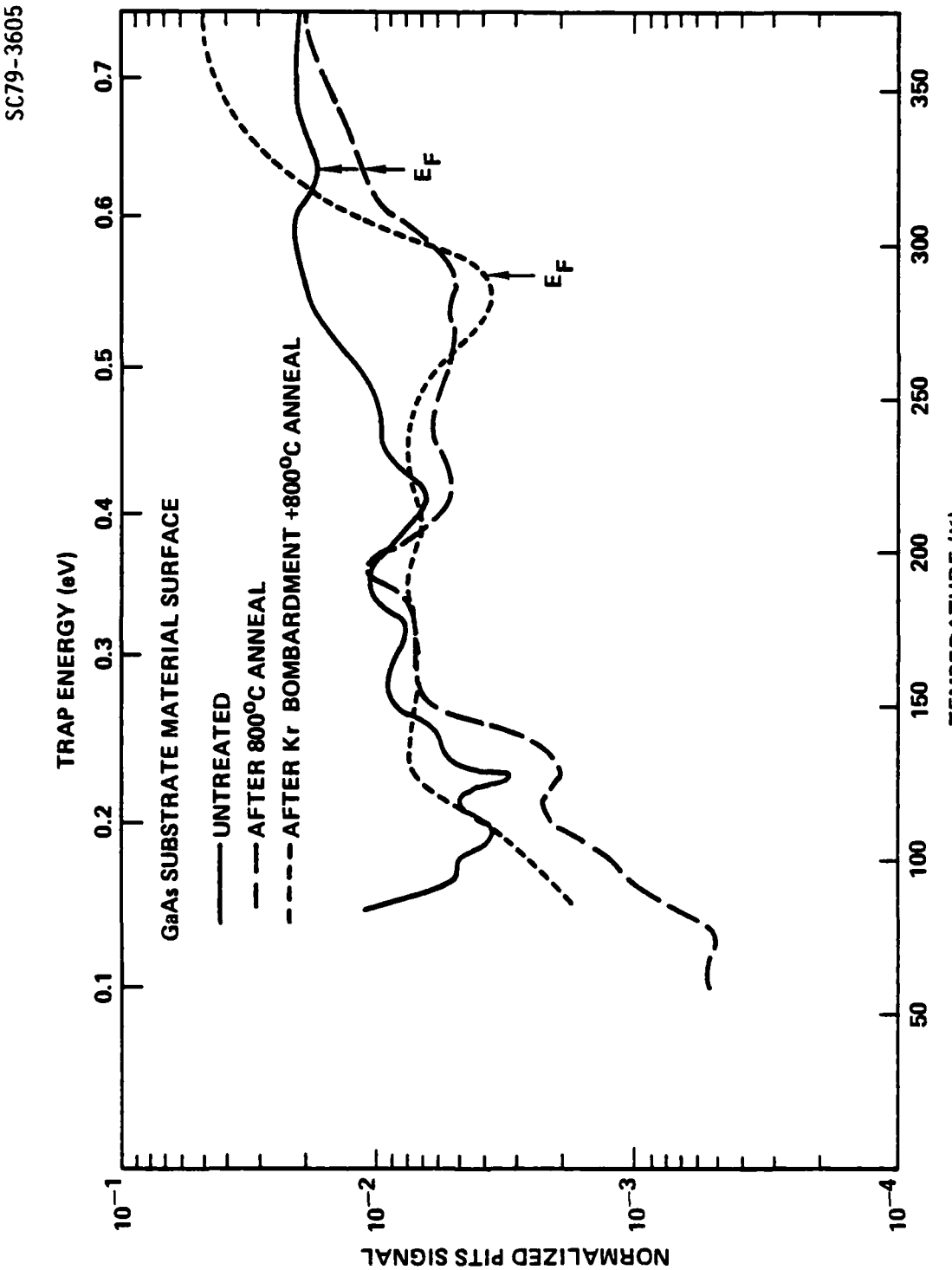

Fig. 2.3-1 PITS spectrum for a specimen of semi-insulating GaAs grown by Morgan Semiconductors.

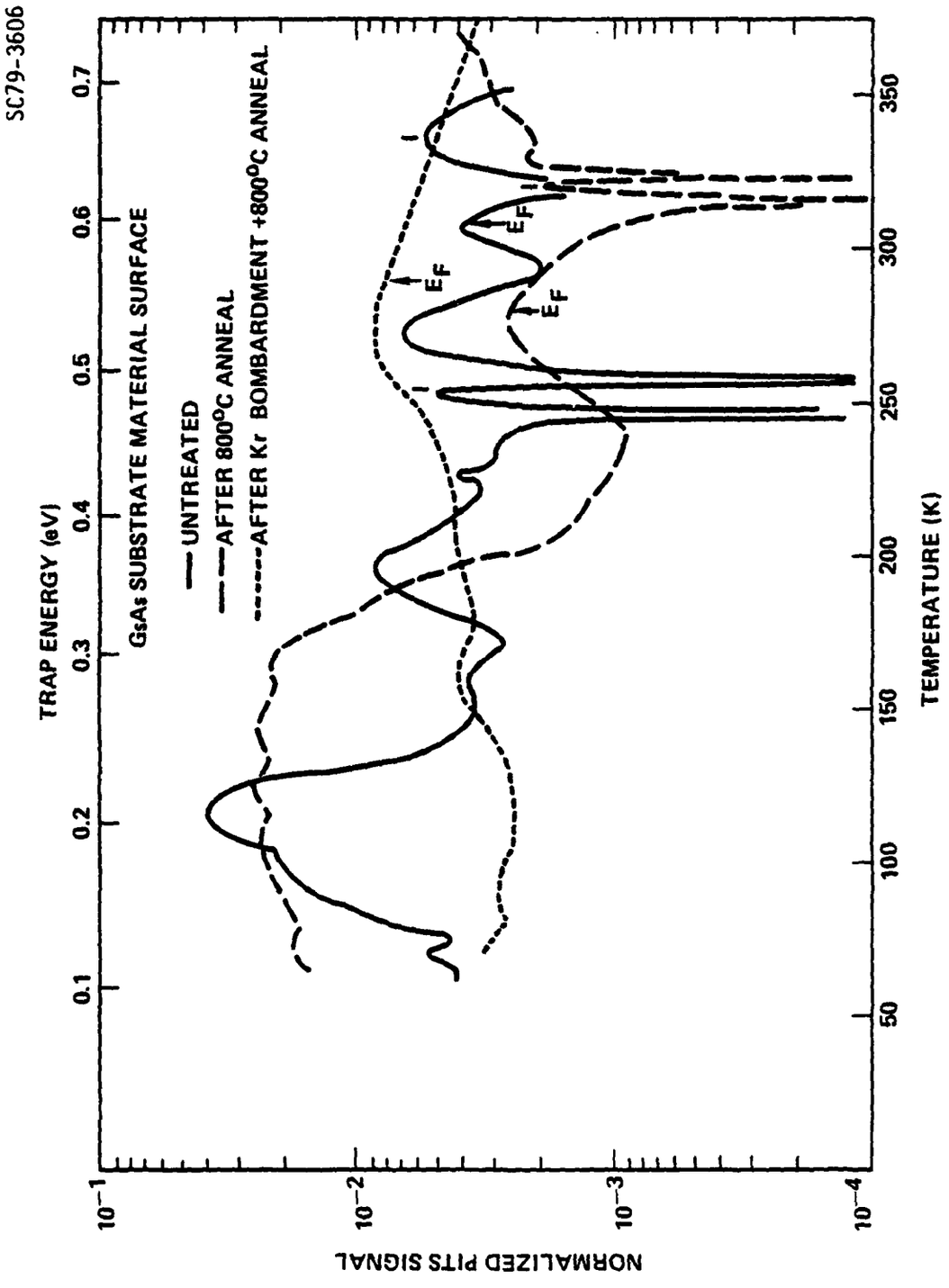

Fig. 2.3-2 PITS spectrum for a specimen of semi-insulating GaAs grown by Crystal Specialties.

Figure 2.3-1, for the Morgan substrate, shows three regions where a significant (although not drastic) change has occurred due to processing. The concentration of shallow traps, < 0.2 eV, and deeper traps, 0.5 to 0.6 eV, has been decreased by the anneal. In the region around mid gap, 0.7 eV, where the recombination centers are located, the concentration of these centers has increased after the bombardment process but not after the anneal. Bombardment also has made the material more n-type, as indicated by the Fermi level which has moved from 0.62 eV up to 0.56 eV from the conduction band.

The Crystal Specialties substrate, Fig. 2.3-2 is very different from the other substrate. The untreated specimen has a higher concentration of shallow traps around 0.2 eV and a higher concentration of low cross section traps, as indicated by the signal inversions, I, at 250K and 335K. The anneal appears to increase the concentration of shallow traps below 0.3 eV and to move E_F from 0.61 eV up to 0.52 eV. The anneal also seems to change the distribution of traps between 0.4 eV and 0.7 eV. The bombardment process homogenizes the trap distribution, reducing the concentration of shallow traps and increasing the concentration of deep traps, and produces a fairly smooth distribution of traps across the bandgap.

These results suggest that PITS constitutes a tool that yields significant information about the response of a particular substrate specimen to process variables.

3.0 PLANAR PROCESS DEVELOPMENT

The planar GaAs IC process under development is currently being used to fabricate circuits using mask set AR2. Fabricated circuits with gate counts of > 60 gates have successfully been demonstrated (see Section 4.1). These results support our process approach. Therefore, no major changes in the direction of the process development are anticipated.

Organization of the process development portion of this program provides for the continuous processing of demonstration circuits; this is conducted in parallel to several other tasks. Section 3.1 covers recent developments in ion implantation. Section 3.2 summarizes the current process results using mask set AR2, and Section 3.3 discusses the recent progress toward development of a dry etching technique for a high yield multi-level interconnect process.

3.1 Ion Implantation (Science Center and Cal Tech)

The investigation of silicon implantation doping of semi-insulating GaAs has been continued in a cooperative effort between Cal Tech and the Science Center. This effort has been focused primarily on obtaining a better understanding of the doping resulting from high implantation doses. Semi-insulating GaAs wafers were implanted at Cal Tech at room temperature with 300 KeV silicon ions to doses ranging from 1×10^{13} to $1 \times 10^{15}/cm^2$. The samples were then capped with reactively sputtered silicon nitride at the Science Center. Annealing was carried out for 30 min at 800, 850, 900, or 950°C in

flowing hydrogen. Following removal of the silicon nitride the samples were prepared for Van der Pauw measurements. Profiles of the free electron concentration and the electron mobility were determined at Cal Tech using anodic layer removal techniques.

Free electron concentration and electron mobility profiles for several samples are shown in Fig. 3.1-1. The electron concentration profiles are flat with a maximum free electron concentration of 2 to 3 x $10^{18}/cm^3$. This limit on the maximum electron concentration seems not to be affected by changes in annealing temperature or implanted dose. In the samples implanted with 1 x 10^{15} silicon ions per cm^2, no more than about 20% of the implanted silicon is electrically active. In contrast, electrical activities exceeding 90% were obtained for low dose implants (~ 1 x 10^{13} silicon ions/cm^2) when annealed at a temperature of 900°C.(1)

Several of the profiles in Fig. 3.1-1 show doping at depths well beyond the predicted distribution of the implanted silicon (labelled LSS in the figure). This indicates that there has been extensive diffusion of the implanted silicon, probably during the post implantation annealing. Deep inward diffusion, which reduces the silicon concentration to the observed free electron concentration, could account for the flat electron concentration profiles. It should be noted, however, that the electron mobility in the sample implanted with the dose of only 1.7 x 10^{14} ions/cm^2 is significantly higher than in the samples implanted with higher doses. This mobility difference may be due to a difference in silicon concentration in the different samples. Such an interpretation would imply that the maximum silicon concentration in

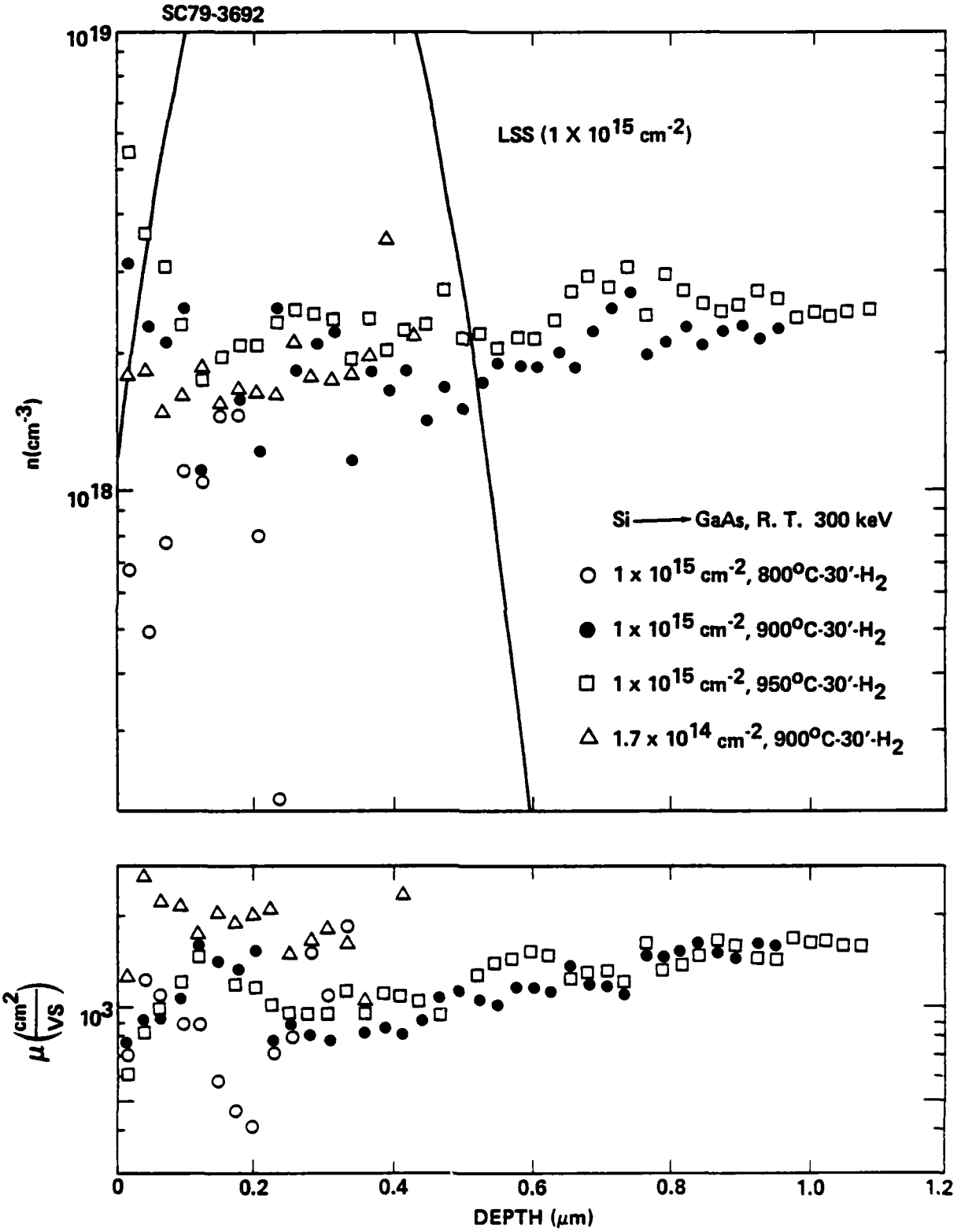

Fig. 3.1-1 Free electron concentration and mobility profiles for semi-insulating GaAs samples implanted with the indicated doses of 300 keV silicon ions and annealed as shown.

samples implanted with doses of 1 x $10^{15}/cm^2$ is well above the measured free electron concentration, and that perhaps the maximum achievable electron concentration is limited to about 2 to 3 x $10^{18}/cm^3$ for the annealing techniques employed in this work (by mechanisms which are unclear at present). Further experiments will be required to determined whether or not there is such a limitation on the electron concentration. The reproducibility of the electron concentration profiles will be verified. A new set of wafers has been implanted with silicon for this purpose as well as to use in completing the coverage of the dose temperature field. Other experiments which could yield useful information include measurements of the silicon concentration over the depth range covered in the electron concentration profiles, and determination of silicon profiles for different implanted silicon doses.

3.2 Fabrication Status (Science Center)

The process technology has been established at the MSI level as evidenced by the fabrication of functioning 64 gate multiplexers.[1,4] The most recent work in the circuit processing portion of the program has concentrated on using mask set AR2 which contains several MSI circuits.

The overall process results do not single out any critical area that may require special attention. The fall-out of wafers along the process is rather random; for example, a few wafers are rejected because of breakage, occasionally the ohmic contacts are poor; and sometimes a wafer is rejected because of poor Schottky gate definition. Wafer throughput over a longer period of time will be necessary before any trends can be recognized.

One of the most promising elements of the process is the high yield of good ohmic contacts that is being achieved. Excellent ohmic contacts were observed on 85% of the recent AR2 wafers. Typical saturation voltages of 1 - 1.5 V for 4μm source to drain gaps are observed with I_{ds} = 4 - 10mA depending on the individual lots monitored. Although no specific ohmic contact resistance measurements have been made recently, earlier measurements on contacts with similar saturation characteristics resulted in values in the low $10^{-6}\Omega cm^2$ range. Another sensitive indicator of good ohmic contacts, as well as the quality of Schottky barriers, is the high yield and low series resistance of the small 1μm x 2 μm Schottky barrier diodes.

Active layer control is probably the major issue for the reproducibility of circuits that require low threshold voltage characteristics. As shown in previous reports, very small changes in device active layer carrier concentration profiles result in significant FET pinch off voltage variations. An example of this is shown in Fig. 3.2-1. These profiles were from measurements made on parallel test chips corresponding to three AR2 lots. Each subsequent lot has a slightly higher implantation dose; this results in slightly different profiles and reflects increasingly higher depletion voltages. A range of doses is normally used on different process lots so that a useful spread of power levels can be evaluated during early stages of our circuit development. FETs monitored from Lot 1, with the lowest implantation dose, resulted in devices characterized by 0.6 - 1 V pinchoff voltages with I_{dss} in the 1 mA range. In contrast, FETs from Lot 3 had significantly higher pinchoff voltages (~2 V). One should note that these voltages were higher than the

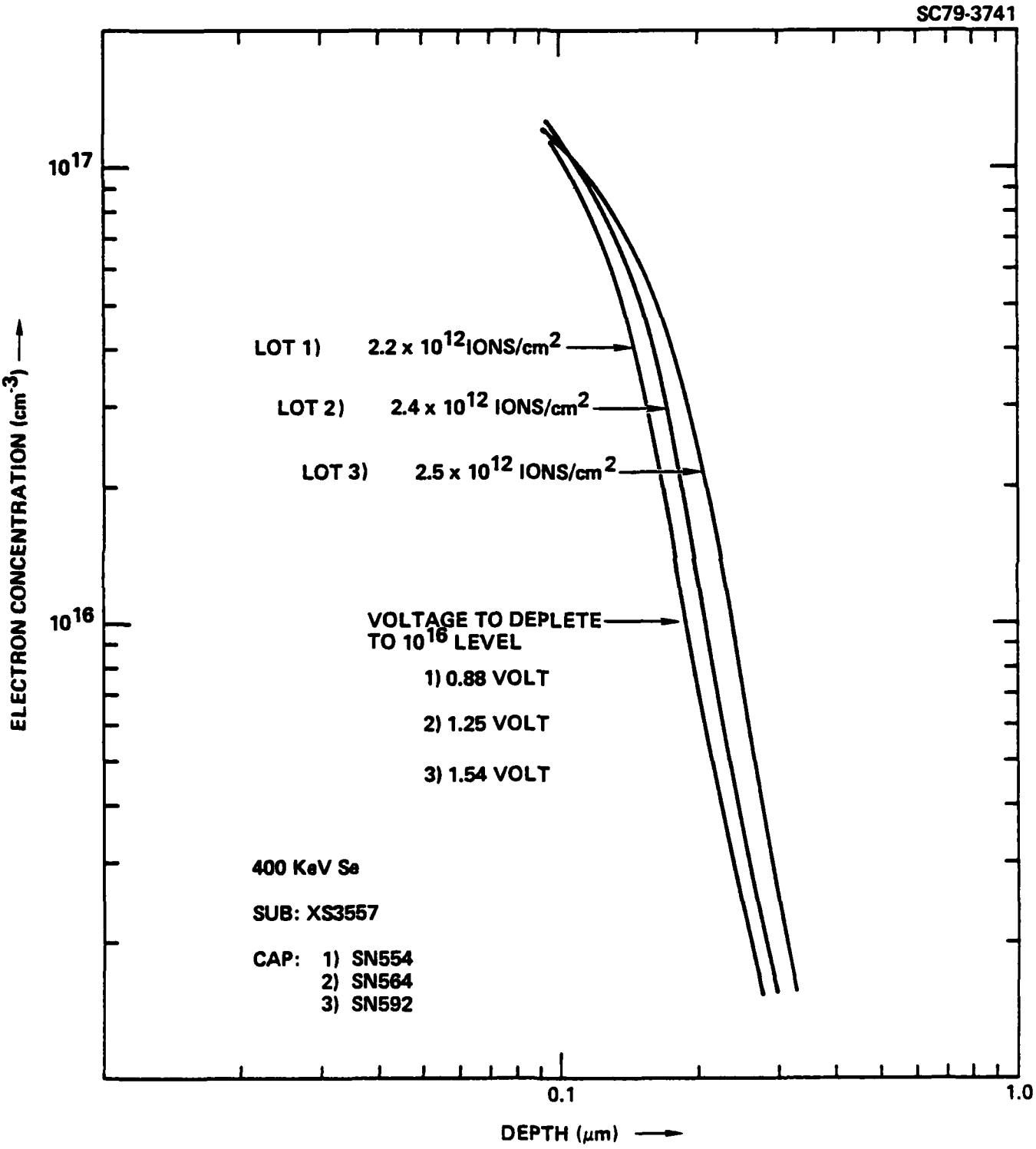

Fig. 3.2-1 Carrier concentration profiles measured on parallel test chips from GaAs IC AR2 lots 1-3 showing the voltages required to deplete these layers to a $10^{16}cm^{-3}$ level.

test chip profile indicated. In general, the parallel test chips are a reasonably good guide to what can be expected on the actual circuits; however, since the IC wafers undergo a more complicated process, other factors may be influencing the resulting device parameters. A better monitoring method will be available in the near future when the on chip automatic C-V profile analysis system is completed.

3.3 Multi-Level Interconnect Process (Science Center)

The currently used photoresist lift-off technique for delineating the second level interconnects has several limitations. Because of the basic nature of a lift-off technique, it is necessary to limit the metalization thickness to 3000Å in order to ensure a high yield process. This use of thin metal interconnects results in certain disadvantages. First, the voltage drop along power bus lines can be appreciable causing poor circuit performance. Second, in order to maintain good via hole step coverage, the 2nd level dielectric (Si_3N_4) must also be thin (~3000Å). Since the crossover capacitance is inversely proportional to the Si_3N_4 thickness, it is desirable to increase the Si_3N_4 thickness in order to obtain smaller crossover capacitance. Based on these considerations, an etching technique is under development. Such technique will allow the use of thicker metal and Si_3N_4 films, while still providing excellent circuit process yield.

Chemical etching was not considered an acceptable method because of the fine line requirements of GaAs ICs. As discussed in the Phase I final report,[1] several dry etching techniques are available, including ion

milling, sputter etching, reactive ion etching, and plasma etching. Sputter etching and reactive ion etching were not considered since they operate at pressures of several mTor, and the substrates are exposed to a plasma environment that may damage the devices because of ion bombardment. Because little was known about the application of plasma etching to Au based metalizations, this approach did not appear to be an attractive choice. Ion milling was chosen because it is a field and plasma free process, and it is conducted in a high vacuum environment ($\sim 10^{-4}$mm Hg). Also, since ion milling is not a chemical process, any material can be etched without difficulty.

A Commonwealth Scientific Millatron II is used for ion milling. The machine is capable of doing both ion milling and ion beam coating. The samples can be milled at a pressure of 1.5×10^{-4} Tor or lower. Samples are mounted on a water cooled stage which can be rotated around its axis and simultaneously translated back and forth along the stage plane. The rotation assures that no shadowing or buildup of surface defects will occur as a result of unidirectional milling. The translation tends to average out nonuniformities in ion beam current density. The type of ion beam selected, along with current, energy and angle of incidence, can be chosen independently for any given application. The beam reaching the substrate can be electrically neutralized so that surfaces do not become positively charged and repel or distort the ion beam.

Both the conventional lift-off process and the experimental ion milling process are now alternatively used in defining the second-level interconnects. As described in the Phase I final report,[1] the proces

sequence using plasma Si_3N_4 starts after completion of first level interconnects, once the devices and circuits are dc tested and receive a process go decision. The wafer is cleaned with a low energy O_2 plasma in order to remove any organics and to prepare the surface for adherence of the plasma Si_3N_4 film. A 3000Å layer of Si_3N_4 is deposited on the GaAs ICs at a temperature of ~300°C. A photoresist pattern defines the via window openings that are required for connecting the first level interconnects to the second level interconnects. Via holes are plasma etched through the Si_3N_4 layer down to the underlying Au interconnect which serves as an automatic etch stop. If the lift-off technique is used, the via hole step is followed by the second level interconnect photolithography step, and the metal evaporation and lift-off steps. If the ion milling technique is used, the via hole step is followed first by the evaporation of second level interconnect metal and, second by the photolithography step. The mask used in the ion milling process is the inverse of that used in the lifting process. After the photolithographic step, the desired pattern of second level interconnects is defined with photoresist, and the unwanted portion of metal film is removed by ion milling. The circuit fabrication is completed by removing the remaining photoresist. On samples prepared for the experimental ion milling process, a 3000-5000Å Ti Au layer is currently being used. The Pt barrier layer has been omitted in order to simplify the initial ion milling experiments.

Angle of incidence is an important parameter in ion milling. It can be chosen to give the maximum etch rate, to give a maximum differential etch rate between materials, or to control the sidewall slope of etched features.

Experiments varying the angle of incidence vs etch rate have been carried out on various materials common to our process. The etch rates of Au, Ti and Si_3N_4 at various angles of incidence are shown in Fig. 3.3-1. The angle of incidence is measured between the incident ion beam and substrate surface plane. Both Ti and Si_3N_4 have low etch rates at 90° incidence. The etch rate increases when the angle of incidence is reduced, and reaches a maximum at an angle of ~40°. It later decreases as glancing angles are approached. In contrast, the etch rate of Au was found to decrease first and later increase as the angle of incidence decreases. Our measured etch rates are somewhat different from other workers results, but a different energy was used in their experiments.(5)

The etch rate ratio of Au to Si_3N_4 is maximum at a 90° angle of incidence. This indicates that the short extra milling period, which is necessary to ensure that metals are completely etched through, will not etch the Si_3N_4 to any great degree provided a 90° angle of incidence is used. The net redeposition rate of etched material also depends on the angle of incidence. We will continue the experiments on optimizing the angle of incidence for ion milling the second level interconnects.

Photomicrographs of a sample after ion milling are shown in Fig. 3.3-2(a) and (b). In Fig. 3.3-2(a) the ion milled sample has photoresist remaining on top of the second level metal, while in Fig. 3.3-2(b) the photoresist has been removed. Performance characteristics of a typical planar FET from this wafer before and after the ion etching of the second level

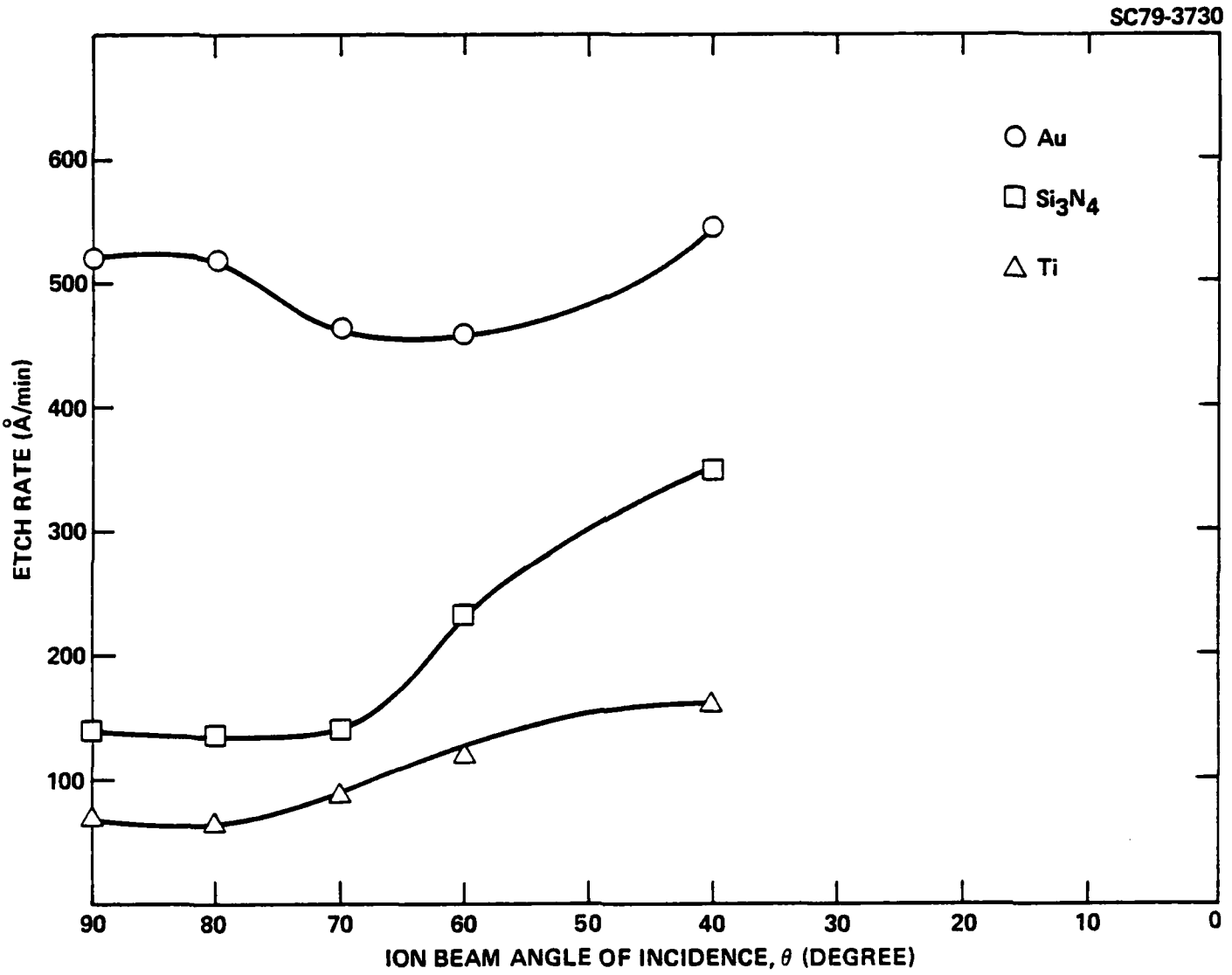

Fig. 3.3-1 Etch rate vs. angle for 800V argon ion beam milling.

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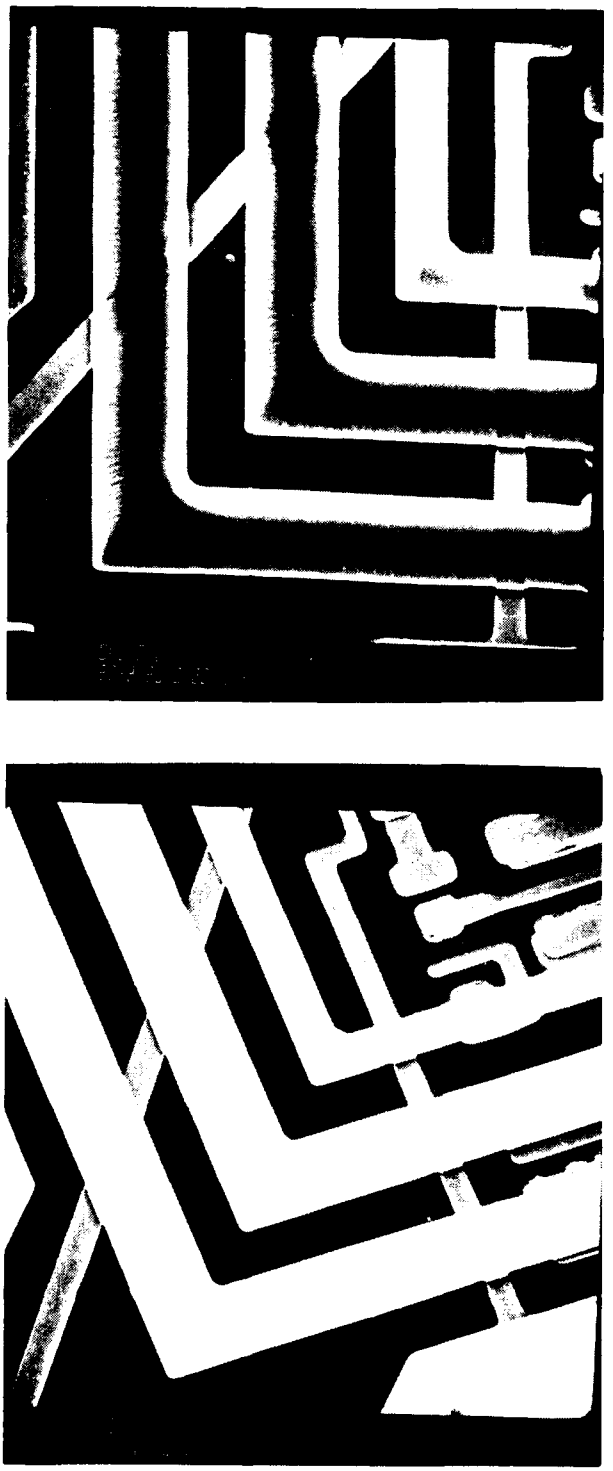

Fig. 3.3-2 Photomicrographs of portions of circuits on wafer showing second layer metallization lines fabricated using ion milling.

interconnects are shown in Fig. 3.3-3. The dc I-V characteristics for these planar FETs (50μm wide and 1μm long gate) remain unchanged after this process.

Although the initial experiments have shown that ion milling is a suitable technique for delineating the second level metal, several elements of the process still need to be refined. Unlike the plasma etching of Si_3N_4 via windows which stops automatically at the underlying Au, the ion milling process must be terminated manually when the unmasked metal film has been etched off completely. This is currently done by knowing the metal film thickness and etching rate, and estimating the time required to etch off the metal film. An alternative method takes into consideration reports that Ti/W films exhibit a blue glow when ion bombarded with Ar. Ti/W films will be evaluated in order to determine whether the glow during ion milling can be used as a visual indication of the complete etch of Au. It is anticipated that the remaining Ti/W would be plasma etched. The trade-offs of this added step must be evaluated. More reliable end-point detection methods, such as mass spectroscopy, are also under consideration. Mass spectroscopy can precisely indicate the end-point by monitoring the appearance of Si signal that comes from the Si_3N_4 under the second level metal.

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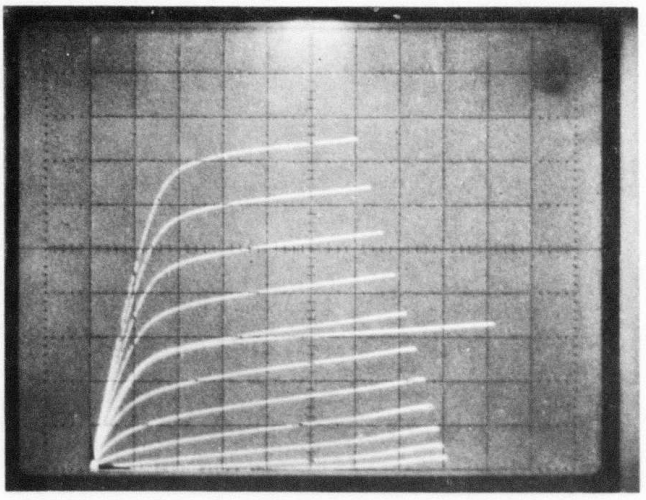
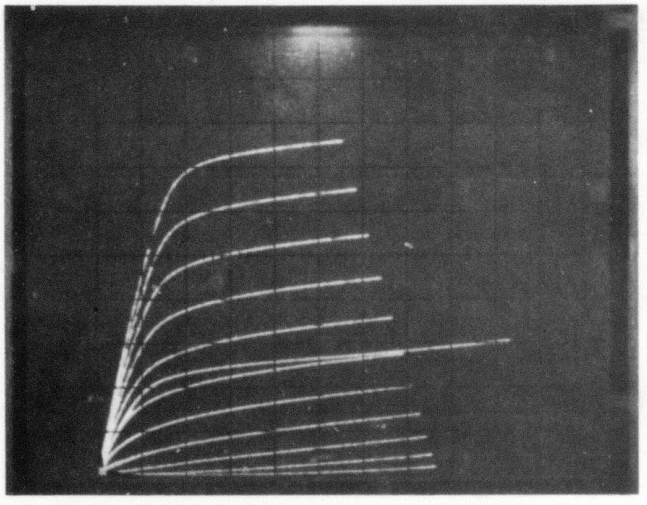


Horiz: 0.5V/div
Vert : 1mA/div
0.2V/step



Horiz: 0.5V/div
Vert : 1mA/div
0.2V/step

Fig. 3.3-3 I-V characteristics of an FET measured before and after the second layer metallization process carried out using ion millings.

4.0 CIRCUIT PERFORMANCE AND DESIGN

Testing of MSI circuits has been very successful. Proper operation of a multiplexer employing 64 gates has been demonstrated. This multiplexer, reaching into the MSI range, is the most complex GaAs IC built to date. Results on multiplexer evaluation are presented in Section 4.1, along with some results from the evaluation of National Bureau of Standards (NBS) semiconductor test patterns, and with some conclusions from the statistical analysis of test device data acquired with our automatic measurement system. A new mask, AR3, is being designed. The organization of this new mask, as well as the type of circuits and test pattern that it will contain, is discussed in Section 4.2. Finally, recent results from FET modeling at Cornell University are presented in Section 4.3.

4.1 Device and Circuit Measurements (Science Center)

This section covers: first an evaluation of some National Bureau of Standards (NBS) test patterns for measurement of sheet resistance and linewidth, and for the electrical measurement of alignment between mask layers; second, the result of statistical correlation analysis of FET parameters; third, data demonstrating the operation of the 64 gate multiplexer.

4.1.1 NBS Test Patterns (Science Center)

The National Bureau of Standards has been very active in the development and analysis of test patterns for the evaluation of material quality and process steps in semiconductor technology.[6] Although all of the NBS efforts have been directed toward silicon technologies, some NBS test patterns can be used in our GaAs technology. This is the case for sheet resistance and linewidth,[7] and for electrical alignment test patterns.[8] These test patterns were incorporated into mask set AR2 for evaluation.

Figure 4.1-1 shows the result of comparing a cross-bridge sheet resistance-linewidth NBS test pattern (bottom right of the figure) with a conventional Van Der Pauw test pattern (top right of the figure). Both patterns have been used on n^+ (sulfur implanted) layers. The top and center oscilloscope pictures show a comparison (from the same wafer) of measurements on these test patterns. The voltage drop between contacts D and C is displayed against the value of the current passing between contacts A and B. The values of the sheet resistances, 465 Ω/□ for the conventional test pattern and 477 Ω/□ for the NBS test patterns, agree within the measurement error (the difference is only 2.5%). Although the NBS has already demonstrated the validity of the cross-bridge test pattern, this comparison is significant because the n^+ layer exhibits lateral diffusion, and the effect of this diffusion on the measurement accuracy has not been yet investigated at NBS. Incidentally, the oscilloscope pictures shown in Fig. 4.1-1 show four superimposed traces, corresponding to measurements on the same test pattern on four locations over the wafer. This is a good indication of the uniformity of sheet resistance observed over the wafers.

SC78-2697

PD51 SHEET RESISTANCE AND LINEWIDTH FOR n^+ LAYERS.

AR2-33

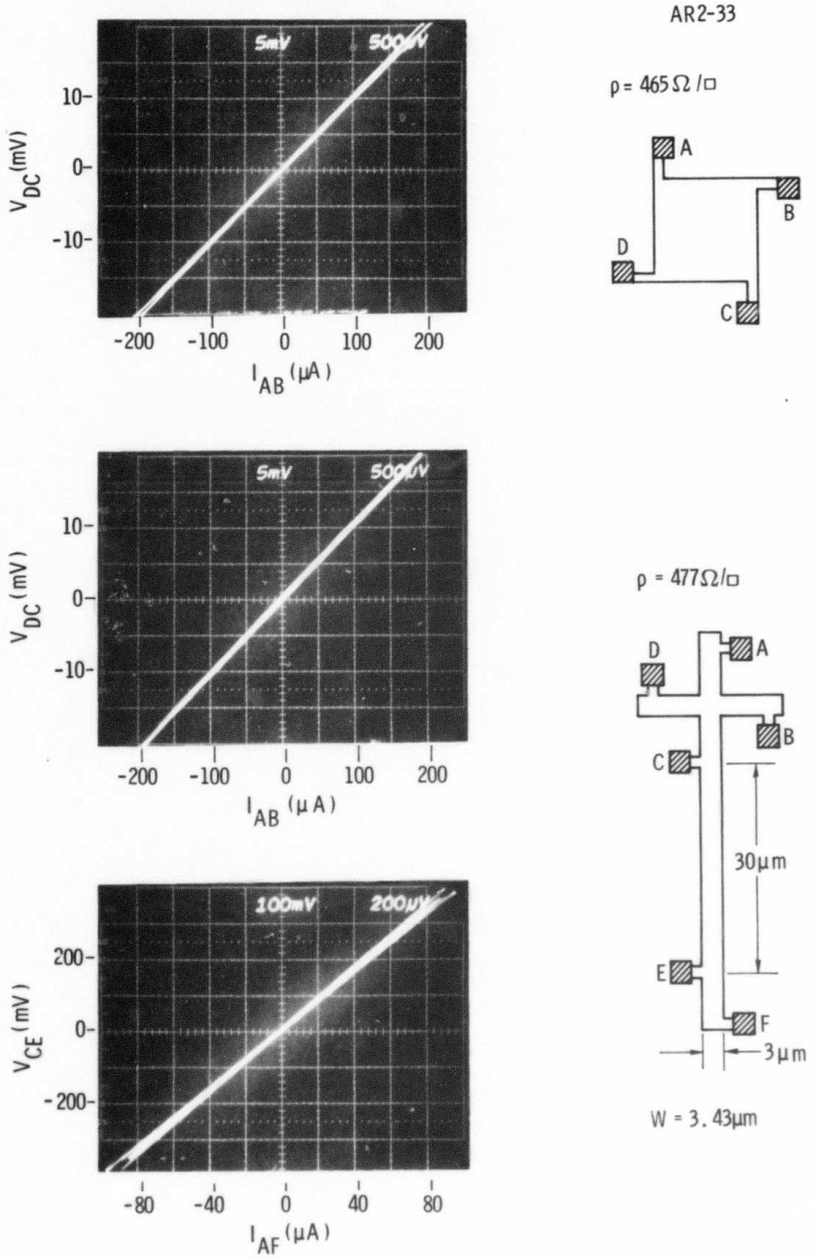


Fig. 4.1-1 Comparison of sheet resistance measurements using a conventional Van der Pauw pattern (top oscillogram) with an NBS cross test pattern (center). Also shown is the result of a linewidth measurement (bottom) using the bridge portion of the NBS test pattern.

The oscilloscope picture at the bottom of Fig. 4.1-1 corresponds to a measurement on the bridge section of the NBS test pattern. Knowing the distance between contacts C and E and the sheet resistance, the linewidth can be calculated from the measured resistance between C and E. The value obtained, 3.43µm, indicates a lateral diffusion of 0.21µm on each side of the nominal 3µm line; a value quite in agreement with the typical diffusion in depth of sulfur implanted layers.

An NBS electrical alignment test pattern is being evaluated. In this test pattern a masking step places a small contact in the middle of a long conductive line built with a different mask step. How well the contact is centered is measured by voltage differences. This test pattern can be used only for verifying the relative alignment of electrically conducting layers. In mask AR-2 the test pattern has been implemented in order to verify the alignment of the ohmic contacts with respect to the n+ implants, and of the Schottky metal lines with respect to the ohmic contacts. While the first test, ohmic/n^+, seems to function properly and has a resolution on the order of 0.1µm, the alignment test pattern between first layer metal and ohmic contact was not useable because of the lack of integrity of long thin ohmic contact metal lines. These lines had electrical interruptions, probably due to the ohmic contact metal being very thin. Note that this observation has no bearing on the practical use of ohmic contact metal in circuits, where the ohmic contact metal is almost completely covered by a layer of Schottky metal. As to the test pattern, this will be reversed in the next mask set so that a small ohmic contact will be centered over a long Schottky metal line.

4.1.2 Statistical Analysis of Device Parameters (Science Center)

The phase I annual report contains a description of the automatic measurement system used for the acquisition of low frequency characteristics of test FETs and diodes, and for their analysis and the display of parameters by wafer maps and histograms.(1) This facility is used for monitoring of device parameters on a routine basis, as a vital part of process evaluation. This capability will gradually be expanded to incorporate more tests, with the final goal being a fully automatic process monitoring system. In addition to the standard application described, the accumulation of a large amount of device parameters over many wafers on computer files offers the opportunity to perform some statistical analysis. This section contains an analysis of the correlations between FET parameters.

Figure 4.1-2 displays saturation current (IDSS) vs pinchoff voltage (-VP) of all the 50 micron wide 1 μm gate test FETs on three wafers. Each wafer corresponds to a cluster of points in the figure. The wafers were chosen so that they exhibited a relatively wide range of pinchoff voltages. The cluster of points near the center of Fig. 4.1-2 corresponds to a standard IC implant profile with a pinchoff voltage slightly above 1V. The other two wafers have a rather high pinchoff voltage, almost 2V, and a very low pinchoff voltage, 0.5V average, respectively. The figure shows very strong correlation between saturation current and pinchoff voltage for the data points. Since variations of saturation current can be caused by a variation of the implantation profile (which also controls the pinchoff voltage) or by other process parameters (e.g., ohmic contact resistance, gate length, etc.), the strong

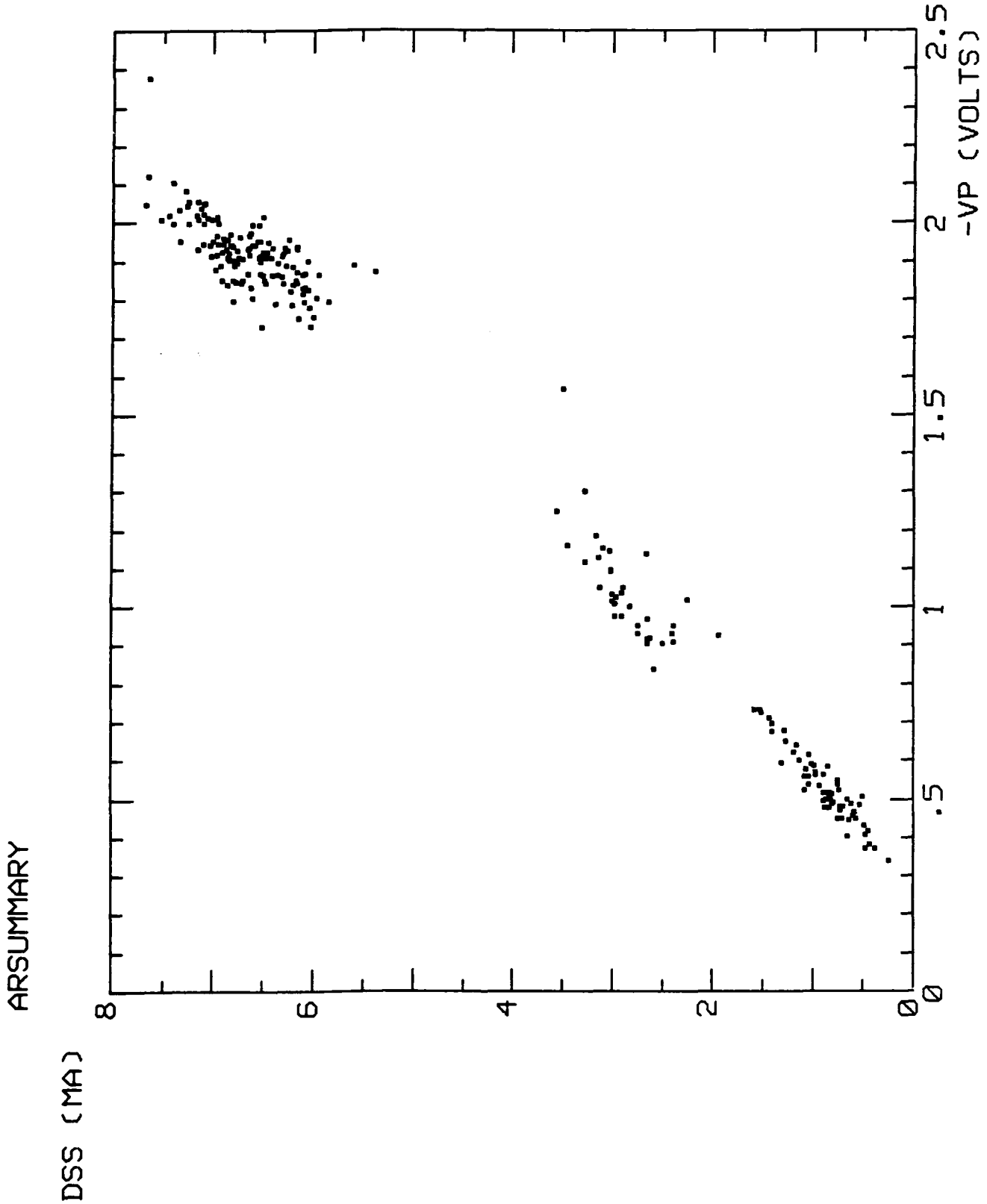


Fig. 4.1-2 Saturation current vs. pinchoff voltage for all the test FETs (50μm wide, 1μm gate) on three test wafers with three ranges of pinchoff voltage.

correlation between saturation current and pinchoff voltage indicates that the relatively small dispersion of saturation current is mainly determined by the dispersion of implant profile characteristics. The other process variables having a smaller effect indicates good process control.

Figure 4.1-3 shows the correlation between on-resistance (RON) and pinchoff voltage (-VP) for the medium and high pinchoff voltage wafers of Fig. 4.1-2. The data points for the high pinchoff wafer show very little correlation between on-resistance and pinchoff voltage. This indicates that for a high pinchoff voltage and, therefore, a relatively deep channel small variations of doping profile have little effect on the on-resistance. On the medium pinchoff voltage wafer there is strong correlation between on-resistance and pinchoff voltage because the thinner channel makes the effect of variations of channel conductance dominant. Altogether, the data points for the two wafers fall on a curve that looks approximately like a hyperbola. Since in first order approximation the on-resistance is equal to the inverse of the transconductance at zero volt gate bias, and the transconductance is roughly proportional to the pinchoff voltage, the hyperbolic dependence is reasonable.

Finally, Fig. 4.1-4 shows the correlation between effective saturation voltage (VSE) and pinchoff voltage (-VP) for the high and medium pinchoff voltage wafers of the previous two figures. There is little correlation between saturation voltage and pinchoff voltage for either wafer. However, the trend from wafer to wafer indicates that the saturation voltage tends to decrease with pinchoff voltage. The dependance of VSE on VP appears

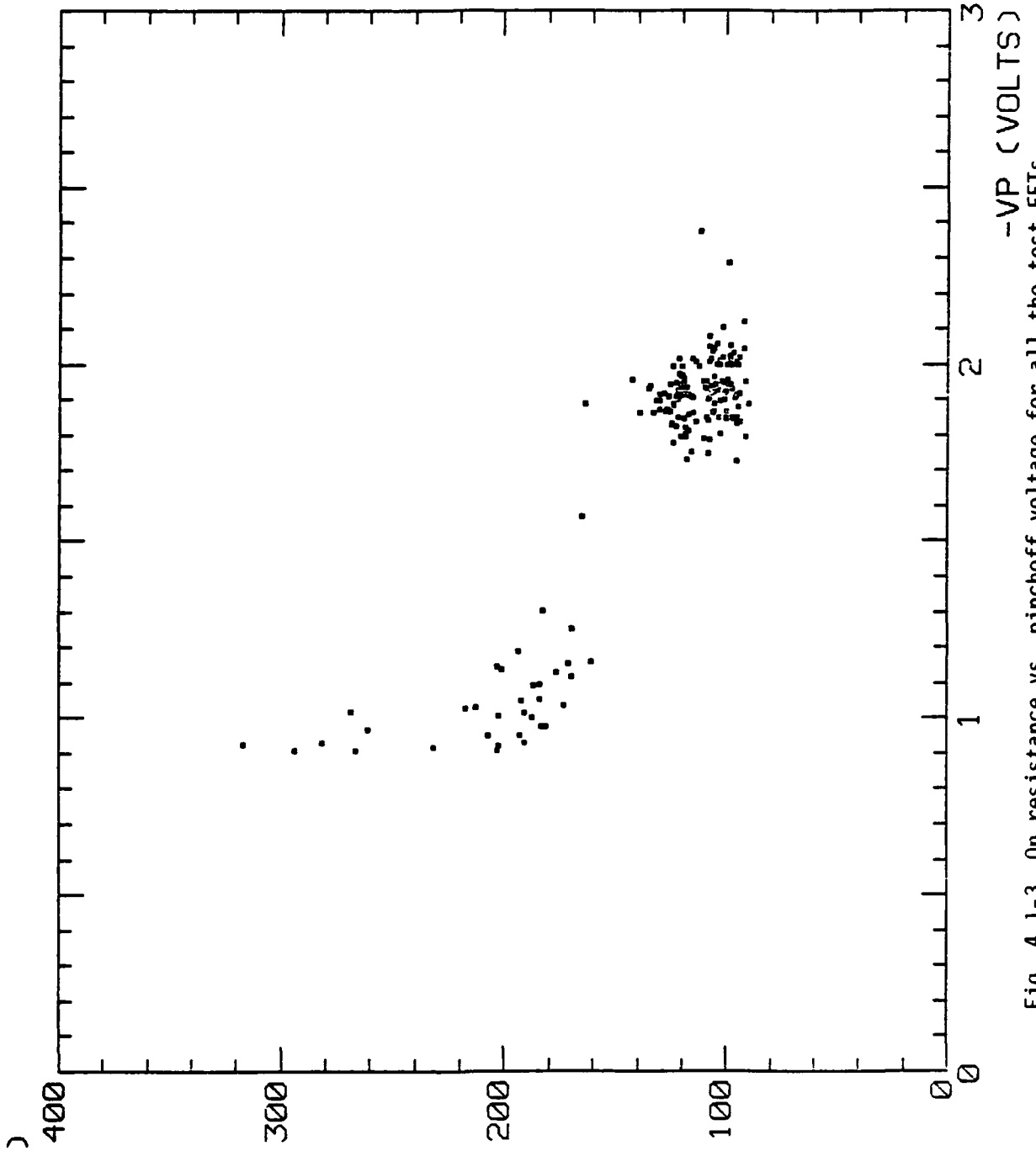


Fig. 4.1-3 On resistance vs. pinchoff voltage for all the test FETs (50μm wide, 1μm gate) on two test wafers with different ranges of pinchoff voltage.

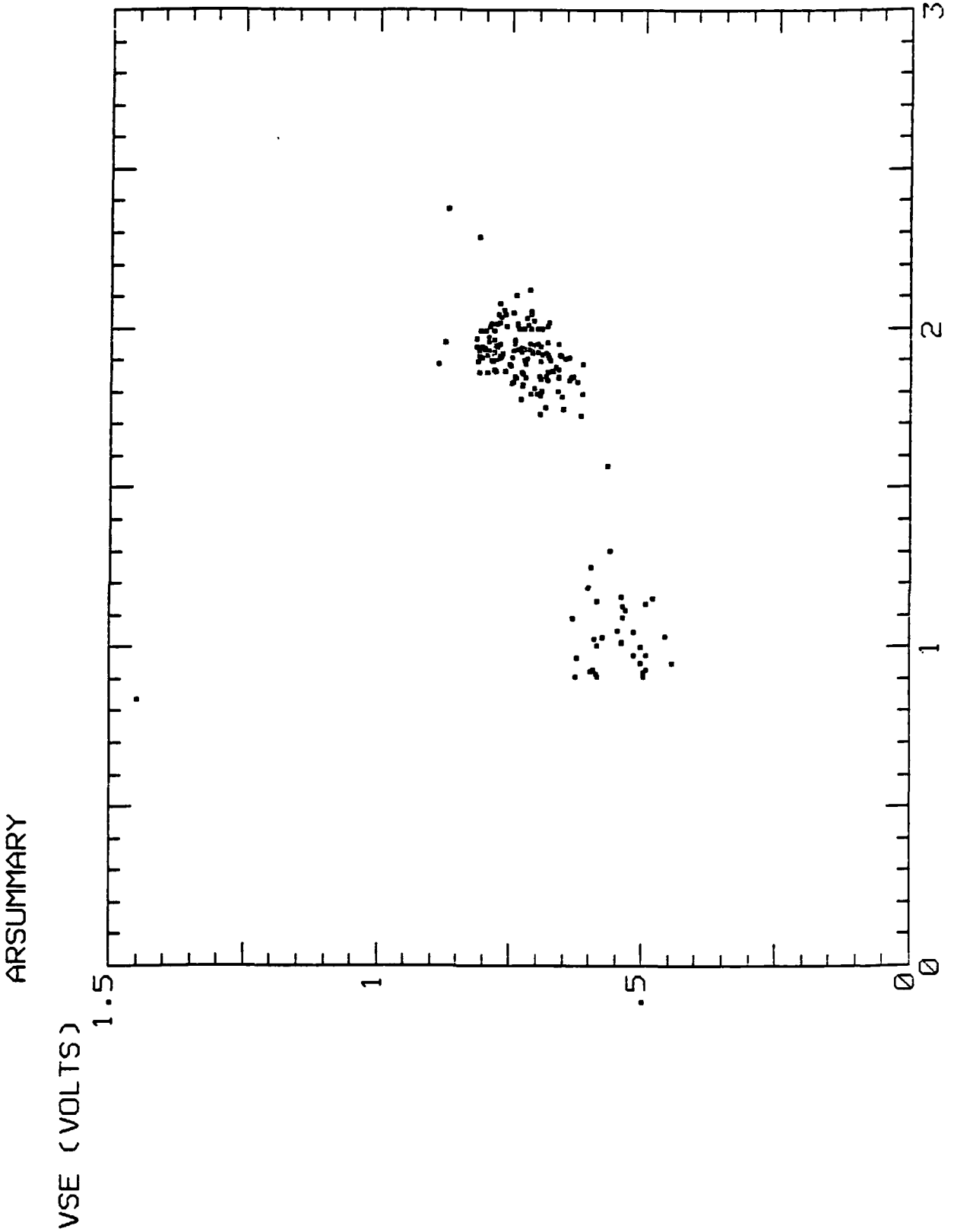


Fig. 4.1-4 Effective saturation voltage vs. pinchoff voltage for all the test FETs (50μm wide, 1μm gate) on two test wafers with different pinchoff voltages.

to be sublinear, probably due to the onset of electron velocity saturation effects in the high pinchoff voltage devices.

4.1.3 Multiplexer Evaluation (Science Center)

Evaluation of high speed circuits was focused on the 8-input data multiplexer during the past quarter. This circuit is designed to switch a single high speed data output from 8 low speed data inputs by selecting one out of eight 4-input NOR gates. The gate selection is carried out on chip with a synchronous counter. All of the circuits required to accomplish this function are implemented using 64 SDFL gates, and are located on one chip (CD11 and CD33 of mask set AR2). This represents the largest GaAs MSI circuit which has been successfully fabricated and tested.

A schematic of the multiplexer circuit is shown in Fig. 4.1-5. The circuit includes a synchronous counter which may be used to generate sequential addresses to the address select portion of the circuit. Two clock enable inputs are provided, so that the clock input to the synchronous counter may be gated on or off. Preset and clear inputs to the counter are provided, so that any address can be set up without having to sequence through undesired addresses. One multiplex input is provided for each of the 8 addresses generated by the counter. A sync output decodes address 000. This output is useful as a reference signal when sequential addresses are generated, and also as an indicator that the counter has been cleared when preset and clear are used for address setup. An additional input is provided for on or off gating of this sync output. This input will be useful when the multiplexer is tested in

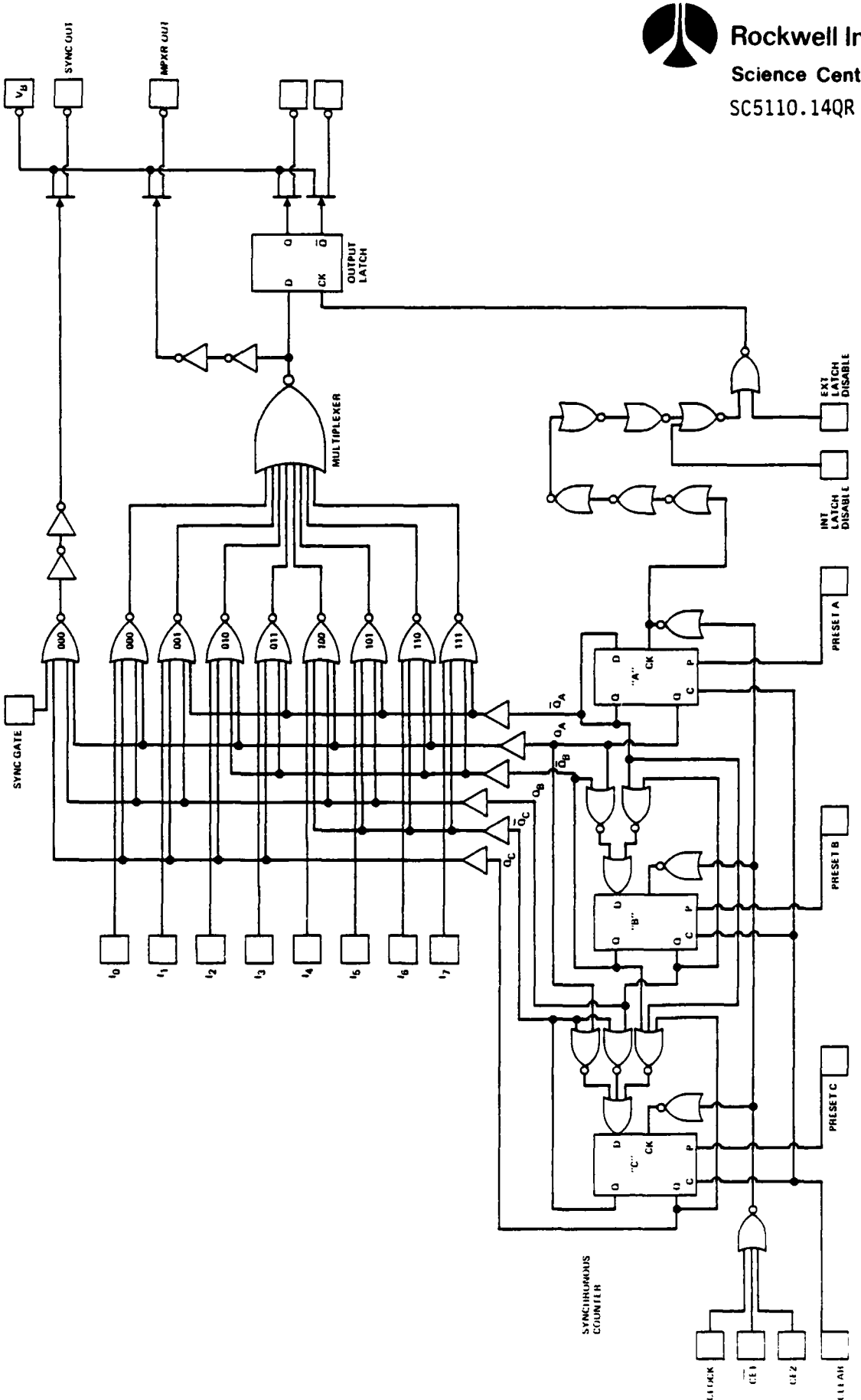


Fig. 4.1-5 Schematic of multiplexer circuit.

conjunction with a demultiplexer. The multiplexed output is also fed into the data input of a D-type latch. This latch may be clocked either from the clock provided to the counter through the appropriate delays, or from a separate input. A separate input is provided for gating the internal clock to the latch. Q and $\overline{Q}$ outputs of this latch are provided. These are useful for observing output data free of unwanted glitches (e.g., when preset and clear are used, the data of address 000 appearing during clear may be undesired) or for simply holding multiplexed data for some extended period of time.

All outputs are buffered by larger FETs connected in the source follower configuration. Their drains are connected together and a separate input (denoted V_B in the figure) supplies drain voltage. This is done because V_B should have a slightly higher voltage than the V_{DD} used for supplying the logic portion of the circuit; it also allows for meaningful power measurements by separating the power dissipation of the logic segment of the circuitry from the power dissipation of the drivers for the external interfaces.

The measurements on the multiplexer circuit were made by using a high speed probe station. The tests were performed with input clock frequencies as high as 0.25 GHz. A Tektronix PG502 pulse generator was used for generating the input clock signals. Input and output were terminated with 50Ω as close to the wafer under test as possible. Standard Tektronix 7000 series oscilloscopes displayed the data. The multiplexer was tested in the sequential mode. The two outputs observed were the sync output and the multiplexer output.

Some results from the multiplexer evaluation are shown in Figs. 4.1-6 through 4.1-8. The first figure (4.1-6) shows circuit performance measured at

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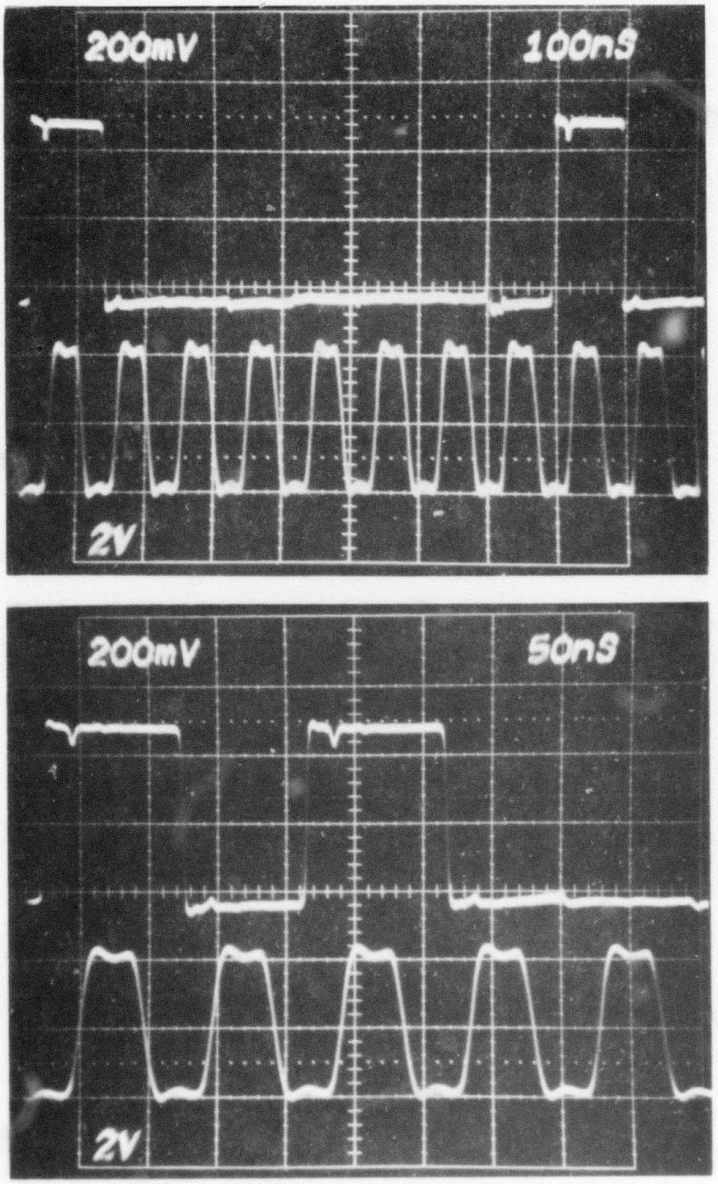

Fig. 4.1-6 Oscillograms showing multiplexer outputs (upper traces) and clock inputs (lower tracers), (a) for one input "high", (b) for two inputs "high".

a relatively low clock frequency (10 MHz) under two input conditions. The upper photograph shows the output with one multiplexer input held high; the lower photograph with two inputs (inputs 3 and 5) held high. This produces a repetitive bit pattern which repeats every eight clock cycles. The two photos in Fig. 4.1-7 were taken on the same chip under the same input conditions, but at higher clock frequencies (as noted in the upper right corner of each photo); 167 and 226 MHz, respectively. The glitch (a spurious, transient output spike) in the top photo is attributed to some possible skew in the outputs of the counter circuitry supplied to the multiplexer select lines. This glitch should not appear in the latched output driven by the "internal" (delayed) clock selected.

The photos in Fig. 4.1-8 depict the sync output of this circuit at two input clock frequencies (254 and 151 MHz). As can be seen, glitches are evident for the same reasons earlier noted. The sync output waveform is useful for monitoring the operation of the synchronous counter during initial adjustment of operating bias and clock levels.

These results mark the first time that a circuit of this complexity (64 gates), using GaAs Schottky diode FET logic, has been successfully tested.[9] The results are very encouraging. Increasing the pinchoff voltage of the FETs should further enhance the high frequency response (the average pinchoff voltage for FETs on this wafer is only 0.53V). However, the low pinchoff voltage accounts for the very low power dissipation of these circuits (as low as 80 mW for the entire circuit.) Testing of wafers which are expected to demonstrate operation at higher speed is in progress.

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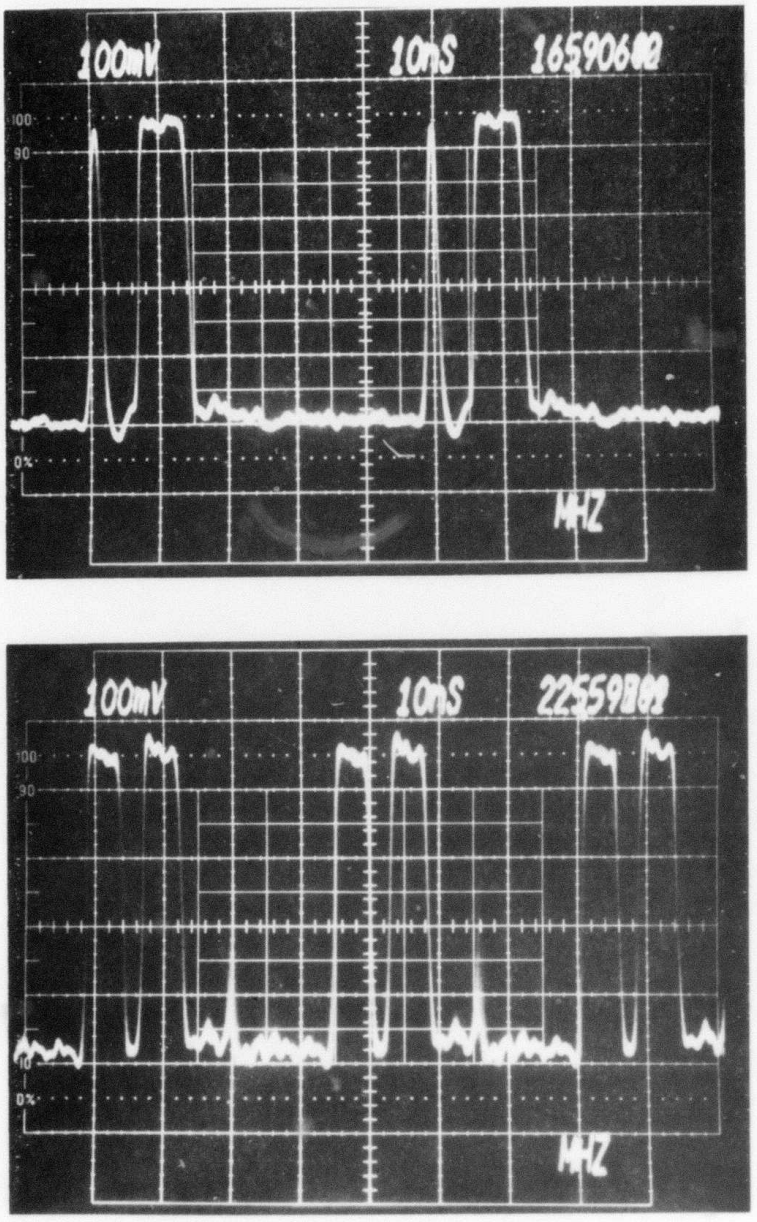

Fig. 4.1-7 Multiplexer outputs (a) for one input "high", (b) for two inputs "high".

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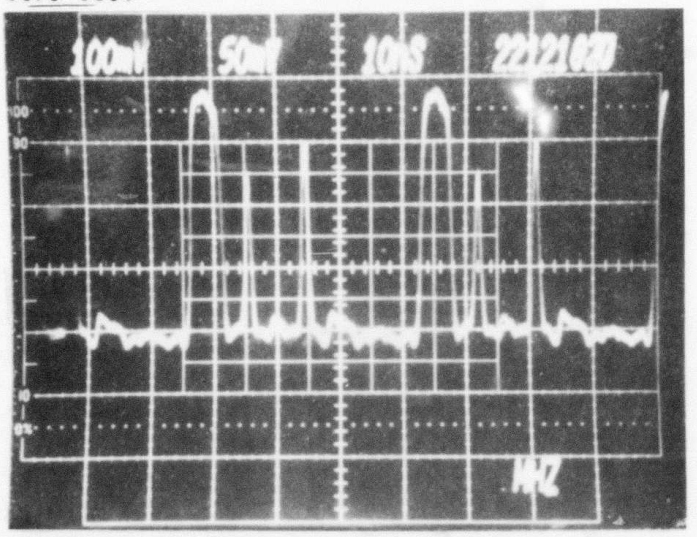

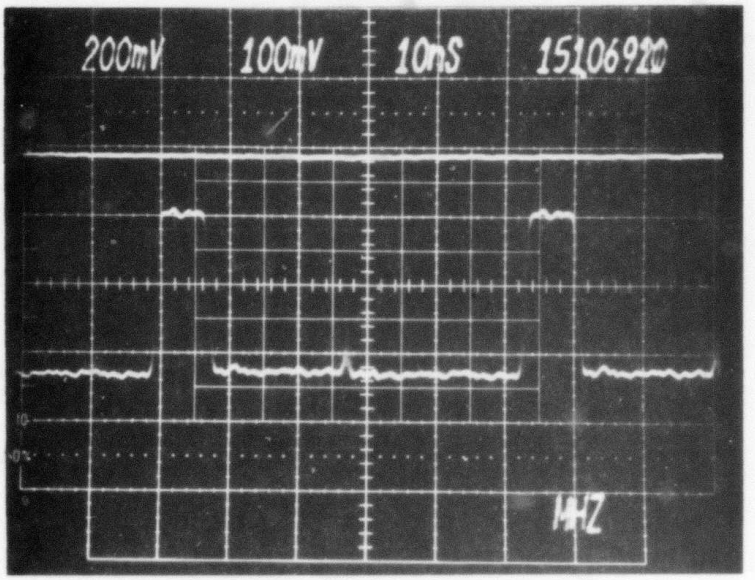

Fig. 4.1-8 Sync outputs of multiplexer circuit corresponding to (a) 253.5 MHz input clock frequency, (b) 151.0 MHz input clock frequency.

4.2 Mask Design (Science Center)

During the first phase of this program, two mask sets were designed and implemented. The first of these, AR1, was directed toward development and evaluation of a planar, SDFL process technology. Planar process uniformity, design rule development and device performance were explored on this first mask set. A maximum circuit complexity of 10 gates was imposed in order to focus most of the effort onto key process and device design considerations. When adequate information had been gained from these test cells and circuits, it was necessary to have a new set of demonstration circuits in order to implement what had been learned from AR1, both in processing and in device design. Therefore, a second mask set, AR2, was designed, digitized and fabricated. This mask included MSI circuits up to a 64 gate level of complexity as well as revised process development test cells.

Circuit evaluation on the AR2 mask set has been carried out, as discussed in Section 4.1 and in previous progress reports. Operation of the 8 input data multiplexer, an MSI circuit with 64 gates, has been achieved. While further evaluation of test cells, multiplexers and the 1:8 data demultiplexer will continue on AR2, design of circuits for a third mask set has been initiated.

The third mask set, AR3, will contain circuits with increased complexity over AR2, including a latched demultiplexer containing more than 100 gates. The basic 9 chip organization, lot size and pad configuration of earlier mask sets will be retained. Because many of the process monitoring and development test cells on earlier mask sets have already been fully

evaluated, the process development (PD) chip included on AR1 and AR2 will be redesigned and merged into the process monitor (PM) chip. The MSI demonstration circuits will be located in a circuit development (CD) chip as was introduced on AR2.

The CD chip will contain four demonstration circuits in the upper MSI level. These circuits are currently being designed and evaluated on a logic simulation computer program. The 8 input multiplexer and 1:8 demultiplexer from AR2 have been redesigned to correct for power bus loading limitations. In addition, the redesigned demultiplexer will include output latches on each of the 8 output lines. Two new circuits are also being designed for AR3. An 8 stage D Flip-Flop shift register/code generator containing approximately 85 gates and a 3 bit-by-3 bit parallel multiplier containing approximatelly 60 gates will also be included on mask set AR3.

4.3 GaAs FET Modeling (Cornell University)

The effort at Cornell University over the last quarter has been concentrated on the role of the substrate current in GaAs MESFETs. It was found that substrate current in GaAs MESFETs may be generated by electron injection into the substrate region adjacent to the high-field domain in the active layer. Because the fringing fields are very high, it was assumed that the injected electrons moved with the saturation velocity. A simple one-dimensional calculation then showed that the substrate current I_{sub} was proportional to $V_{ds}^{1/2}$ and $n_o^{1/4}$ where V_{ds} is the drain-to-source voltage, and n_o is the doping density in the active layer. Estimates also indicate that

the parasitic substrate current degrades the high frequency performance and noise figures for low-noise MESFETs devices.

Efforts to modify the model to include the non-uniform profiles typical for ion-inplanted devices has continued. Integro-differential equations linking the transconductance versus gate voltage curve with the doping density versus distance from the gate curve were derived. The analysis and solution of these equations and an attempt to interpret device data will continue.

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